

M.2 Updates

Manisha Nilange
M.2/Mini WG Chair
IO Architect
Intel Corporation

Copyright © 2017 PCI-SIG® - All Rights Reserved

Disclaimer

The information in this presentation refers to specifications still in the development process. This presentation reflects the current thinking of various PCI-SIG® workgroups, but all material is subject to change before the specifications are released.

Copyright © 2017 PCI-SIG® - All Rights Reserved

Agenda

- **Review changes to the M.2 Specification**
- **Review Post Rev 1.1 Specification Release ECNs**
- **Review main errata items**
- **Review changes to the Mini CEM Specification**
- **Timeline**

Copyright © 2017 PCI-SIG® - All Rights Reserved

Approved ECNs Added to Rev 1.1

- **ECNs Approved Post Rev 1.0 Specification Release:**
 - Transition of NFC Signals from 3.3 V to 1.8 V
 - M.2 COEX Signal Definition - UART
 - SMBus Interface for SSD Socket-2 and Socket-3
 - Power-up Requirements for PCIe side bands (PERST#, etc.)
 - Power-up Requirements for PCIe side bands in a Vbat powered system
 - TX Blanking and SYSCLK on Socket 1 Related Pinouts
 - M.2 Signal Definition – Audio & ANTCTL Functions
 - M.2 2242 WWAN Module
 - Supporting PCIe and SATA BGA form factor SSDs
 - M.2 SSIC Eye Limits Definitions
 - WWAN Key C Definition
- **Errata**

Copyright © 2017 PCI-SIG® - All Rights Reserved

Transition of NFC Signals From 3.3 V to 1.8 V

- **Voltage level of NFC related signals (I2C DATA, I2C CLK and ALERT#) on the connectivity pinouts changed from 3.3 V to 1.8 V**
- **Pinout and voltage definitions changed for Module Key E, Module Key A and Dual Module Key A-E**
- **Socket pinouts updated to reflect this change**

Copyright © 2017 PCI-SIG® - All Rights Reserved

M.2 COEX
Signal Definition - UART

- **Co-existence between WWAN and WiFi/BT**
- **Two COEX signals defined with location of source and sink sides of signal path**
- **Potential interoperability issue resolved**
- **Prevent damage when mix-n-matched**

Copyright © 2017 PCI-SIG® - All Rights Reserved

SMBus Interface for SSD Socket-2 and Socket-3

- **SMBus interface signals added in Socket-2 (SSD) and Socket-3 definitions**
 - N/C signals used for this purpose
- **SMBus Signals defined at 1.8 V**
- **Platform and module pinouts updated accordingly**

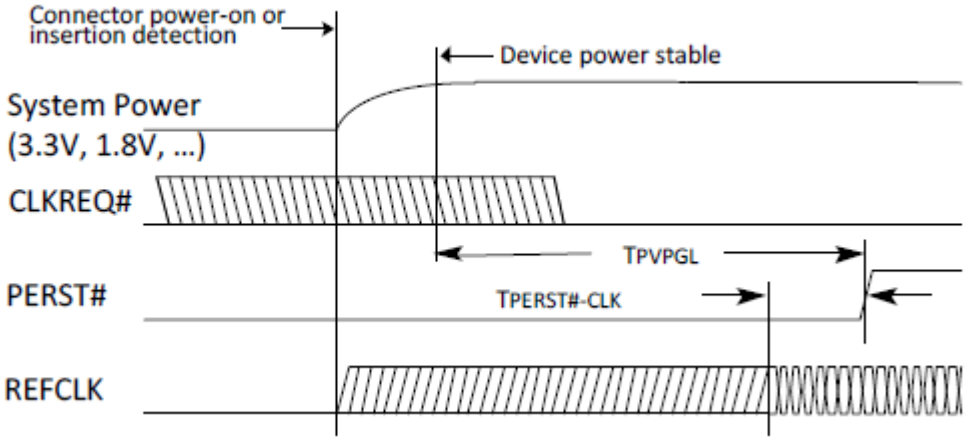
Copyright © 2017 PCI-SIG® - All Rights Reserved

Power-up Requirements for PCIe® Side Bands (PERST#, etc.)

- **Power-up requirements section re-defined to provide more realistic timing model for Reset**
- **PERST# timing variable (T_{PVPGL}) changed to be implementation specific with specific recommended value**
 - Earlier value of 1 ms deemed unrealistic for storage applications.
- **CLKREQ# timing variable (T_{PVCRL}) is moved out of power-up requirements section**

Copyright © 2017 PCI-SIG® - All Rights Reserved

Power-up Requirements for PCIe Side Bands (PERST#, etc.)



Copyright © 2017 PCI-SIG® - All Rights Reserved

Power-Up Requirements for Side Bands in a VBAT Powered System

- **Extends previous ECN, adds timing information for the PCIe start-up of a system powered from VBAT**
- **Clarification added to the definition of FULL_CARD_POWER_OFF#**

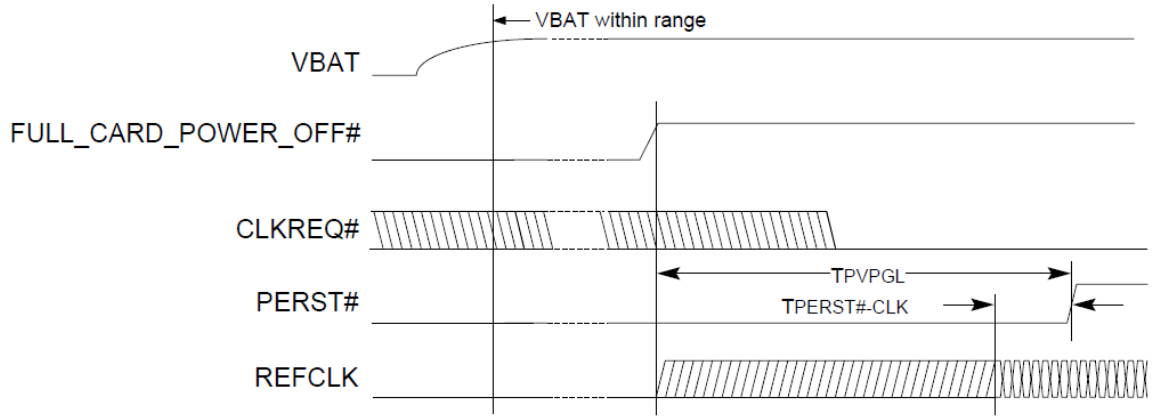


Figure 79b. Power-Up Timing Sequence for a module powered by a direct VBAT connection

Copyright © 2017 PCI-SIG® - All Rights Reserved

TX Blanking and SYSCLK on Socket 1 Related Pinouts

- **Include 2 GNSS aiding signals (TX_Blanking and SYSCLK) in Socket-1 Key-E pinout and Type 2226 and Type 3026 pinout to align with Type 1216 pinout**
- **GNSS aiding signals overlapped with SDIO RESET# and SDIO CLK for Socket-1 Key E**
 - Selection of active functionality need to be defined between vendor and customer in a BTO/CTO manner
- **In Type 2226 and Type 3026, no selection required as TX_BLANKING and SYSCLK replacing the "Reserved" pins**

Copyright © 2017 PCI-SIG® - All Rights Reserved

M.2 Signal Definition – Audio & ANTCTL Functions

- **Definition added for the four Audio Interface pins and the four Antenna Control pins to provide definitive functions assigned to each pin**
 - Interoperability and damage prevention
- **For Antenna Control (ANTCTL[0..3]), two modes of operation supported: GPIO and RFFE**
- **For Audio Interface (AUDIO[0..3]), two modes of operation supported: I2S and SLIMBus**

M.2 Antenna Control		Pin Mode & Function					
Pin #	Pin Name	GPIO Mode			RFFE Mode		
		Function	Direction	Voltage	Function	Direction	Voltage
59	ANTCTL0	GPIO0(LSB)	O	1.8 V[1]	Reserved		
61	ANTCTL1	GPIO1	O	1.8 V[1]	RFFE_SDATA	I/O	1.8 V
63	ANTCTL2	GPIO2	O	1.8 V[1]	RFFE_SCLK	O	1.8 V
65	ANTCTL3	GPIO3(MSB)	O	1.8 V[1]	RFFE_VIO	O	1.8 V

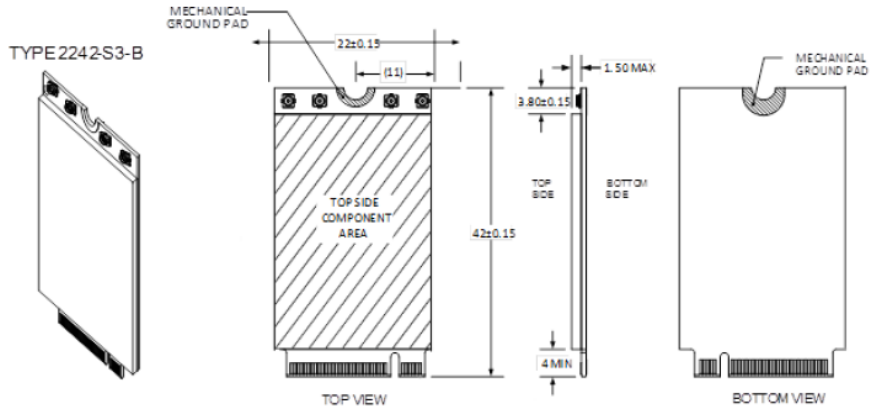
[1] In GPIO Mode Operating voltage for pins is 1.8 V Nominal BUT can be up to 2.8 V to allow direct operation of antenna controllers using multiple silicon technologies.

M.2 Audio Pins		Pin Mode & Function					
Pin #	Pin Name	I2S Mode			SLIMBus Mode		
		Function	Direction	Voltage	Function	Direction	Voltage
20	Audio_0	I2S_CLK	I/O	1.8 V	SLIMBus_CLK	O	1.8 V
22	Audio_1	I2S_RX	I	1.8 V	SLIMBus_DAT	I/O	1.8 V
24	Audio_2	I2S_TX	O	1.8 V	Reserved		
28	Audio_3	I2S_WS	I/O	1.8 V	Reserved		

Copyright © 2017 PCI-SIG® - All Rights Reserved

M.2 2242 WWAN Module

- **Added Type 2242 form-factor for WWAN modules (Socket-2, Key-B)**
- **Driven by desire in the industry to shrink the dimensions for WWAN modules**
- **Backwards compatible with 3042 socket-2 slots**



Note: For card-edge details, see section 2.3.4, Card PCB Details

Figure 10. M.2 Type 2242-S3 Mechanical Outline Drawing Example

Copyright © 2017 PCI-SIG® - All Rights Reserved

M.2 SSIC Eye Limits Definitions

- **Definition of electrical eye limits (Eye Height and Eye Width) at the M.2 connector for SSIC host and device transmitter added as recommendation**

	Eye Height at M.2 Socket	Eye Width at M.2 Socket	Notes
SSIC Device Transmitter	140 mV	0.6 UI_{HS}	1 - 6
SSIC Host Transmitter	95 mV	0.55 UI_{HS}	1 - 6

Notes:

1. Assumes the signal has been captured using a break-out fixture that is approximately 1-inch long (approximately -0.33dB loss @1.455 GHz).
2. The recommended sample size for this measurement is at least 106 UI.
3. Eye measurements require that CRPAT (refer to *MIPI Alliance Specification for M-PHY*) is being transmitted during the test.
4. The measurements are applicable to Terminated HS mode of MPHY.
5. The Eye Width limits are applicable at Target BER of 10-10.
6. The eye limits are applicable to the MPHY HS gears G1, G2 and G3.

Copyright © 2017 PCI-SIG® - All Rights Reserved

WWAN Key C Definition

- **Dedicated WWAN Key C and pinout defined**
 - **Better suited for latest WWAN devices**
 - **New mixture of host interfaces**
 - **1.8 V IO's**
 - **14 vendor defined pins grouped to enable differential and single ended signals in the pinout**

Copyright © 2017 PCI-SIG® - All Rights Reserved

WWAN Key C Definition

Pin	Signal	Signal	Pin
74	3.3 V	GND	75
72	3.3 V	GND	73
70	ANTCTL3 GPIO3 (MSB) (O)/RFFE_VIO (O) (0/1.8V)	RESET# (I) (0/1.8V)	71
68	ANTCTL2 GPIO2 (O)/REF_SCLK (O) (0/1.8V)	COEX_TXD (O) (0/1.8V)	69
66	ANTCTL1 GPIO1 (O)/REF_SDATA (I/O) (0/1.8V)	COEX_RXD (I) (0/1.8V)	67
64	ANTCTL0 GPIO0 (O) (0/1.8V)	GND	65
62	RESERVED	VENDOR_PORT_C_3	63
60	VENDOR_PORT_B_5	VENDOR_PORT_C_2	61
58	VENDOR_PORT_B_4	GND	59
56	RESERVED	VENDOR_PORT_C_1	57
54	VENDOR_PORT_B_3	VENDOR_PORT_C_0	55
52	VENDOR_PORT_B_2	GND	53
50	VENDOR_PORT_B_1	M/REFCKLP	51
48	VENDOR_PORT_B_0	MREFCLKN	49
46	PEWAKE# (I/O) (0/1.8V)	GND	47
44	CLKREQ# (I/O) (0/1.8V)	M/PERp0; SSIC-RxP; USB3.0-Rx+	45
42	PERST# (I) (0/1.8V)	M/PERn0; SSIC-RxN; USB3.0-Rx-	43
40	SIM DETECT2 (I) (0/1.8V)	GND	41
38	UIM2-PWR (O)	M/PETp0; SSIC-TxP; USB3.0-Tx+	39
36	UIM2-DATA (I/O)	M/PERn0; SSIC-TxN; USB3.0-Tx-	37
34	UIM2-CLK (O)	GND	35
32	UIM2-RESET (O)	SIM DETECT1 (I) (0/1.8V)	33
30	AUDIO1 I2S_WS (I/O) (0/1.8V)	UIM1_PWR (O)	31
28	AUDIO1 I2S_TX (O) (0/1.8V)	UIM1_DATA (I/O)	29
26	AUDIO1 I2S_RX (I) SLIMUS_DAT (I/O) (0/1.8V)	UIM1_CLK (O)	27
24	AUDIO1 I2S_CLK (I/O) SLIMUS_CLK (I/O) (0/1.8V)	UIM1_RESET (O)	25
	MODULE KEY C	MODULE KEY C	
	MODULE KEY C	MODULE KEY C	
	MODULE KEY C	MODULE KEY C	
	MODULE KEY C	MODULE KEY C	
20	VENDOR_PORT_A_3	VIO1.8V	15
12	VENDOR_PORT_A_2	FULL_CARD_POWER_OFF# (I) (0/1.8V)	13
10	VENDOR_PORT_A_1	DPR (I) (0/1.8V)	11
8	VENDOR_PORT_A_0	GND	9
6	3.3 V	USB_D-	7
4	3.3 V	USB_D+	5
2	3.3 V	GND	3
		GND	1

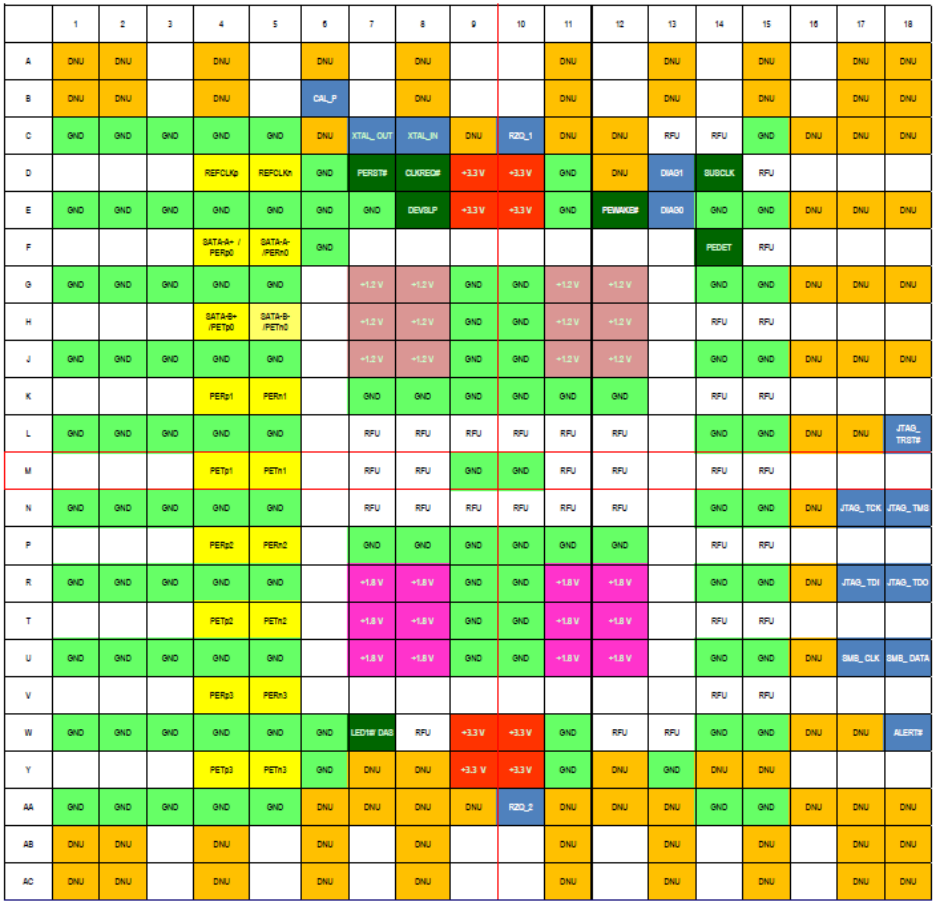
Copyright © 2017 PCI-SIG® - All Rights Reserved

Supporting PCIe and SATA BGA Form Factor SSDs

- **Introduced new family of form-factors and pinouts to allow PCIe and SATA to be delivered using a BGA package**
 - Expands use of PCIe and SATA in small form-factor applications
 - New pinout based on Socket-3 Key-M definitions
 - New pins and voltage rails defined
- **Area savings, lower z-height, better thermals**
- **Type 1620, Type 2024, Type 2228 and Type 2828 defined**

Copyright © 2017 PCI-SIG® - All Rights Reserved

Supporting PCIe and SATA BGA Form Factor SSDs



	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
A	DNU	DNU		DNU		DNU		DNU			DNU		DNU		DNU		DNU	DNU
B	DNU	DNU		DNU		CAI_P		DNU			DNU		DNU		DNU		DNU	DNU
C	GND	GND	GND	GND	GND	DNU	XTAL_OUT	XTAL_IN	DNU	R2D_1	DNU	DNU	RFU	RFU	GND	DNU	DNU	DNU
D				REFCLKp	REFCLKn	GND	PERST#	CLKREQ#	+3.3 V	+3.3 V	GND	DNU	DIA01	SUSCLK	RFU			
E	GND	GND	GND	GND	GND	GND	GND	DEVSLP	+3.3 V	+3.3 V	GND	PEWAKE#	DIA00	GND	GND	DNU	DNU	DNU
F				SATA-A+ / PERp0	SATA-A- /PERn0	GND								PEDET	RFU			
G	GND	GND	GND	GND	GND		+1.2 V	+1.2 V	GND	GND	+1.2 V	+1.2 V		GND	GND	DNU	DNU	DNU
H				SATA-B+ /PETp0	SATA-B- /PETn0		+1.2 V	+1.2 V	GND	GND	+1.2 V	+1.2 V		RFU	RFU			
J	GND	GND	GND	GND	GND		+1.2 V	+1.2 V	GND	GND	+1.2 V	+1.2 V		GND	GND	DNU	DNU	DNU
K				PERp1	PERn1		GND	GND	GND	GND	GND	GND		RFU	RFU			
L	GND	GND	GND	GND	GND		RFU	RFU	RFU	RFU	RFU	RFU		GND	GND	DNU	DNU	JTAG_ TRST#
M				PETp1	PETn1		RFU	RFU	GND	GND	RFU	RFU		RFU	RFU			
N	GND	GND	GND	GND	GND		RFU	RFU	RFU	RFU	RFU	RFU		GND	GND	DNU	JTAG_TCK	JTAG_TMS
P				PERp2	PERn2		GND	GND	GND	GND	GND	GND		RFU	RFU			
R	GND	GND	GND	GND	GND		+1.8 V	+1.8 V	GND	GND	+1.8 V	+1.8 V		GND	GND	DNU	JTAG_TDI	JTAG_TDO
T				PETp2	PETn2		+1.8 V	+1.8 V	GND	GND	+1.8 V	+1.8 V		RFU	RFU			
U	GND	GND	GND	GND	GND		+1.8 V	+1.8 V	GND	GND	+1.8 V	+1.8 V		GND	GND	DNU	SMB_CLK	SMB_DATA
V				PERp3	PERn3									RFU	RFU			
W	GND	GND	GND	GND	GND	GND	LED1# DAS	RFU	+3.3 V	+3.3 V	GND	RFU	RFU	GND	GND	DNU	DNU	ALERT#
Y				PETp3	PETn3	GND	DNU	DNU	+3.3 V	+3.3 V	GND	DNU	GND	DNU	DNU			
AA	GND	GND	GND	GND	GND	DNU	DNU	DNU	DNU	R2D_2	DNU	DNU	DNU	GND	GND	DNU	DNU	DNU
AB	DNU	DNU		DNU		DNU		DNU			DNU		DNU		DNU		DNU	DNU
AC	DNU	DNU		DNU		DNU		DNU			DNU		DNU		DNU		DNU	DNU

= No Solder Ball

Figure 104. Type 1620 BGA Module-side Ballmap (Top View)

Copyright © 2017 PCI-SIG® - All Rights Reserved

Supporting PCIe and SATA BGA Form Factor SSDs

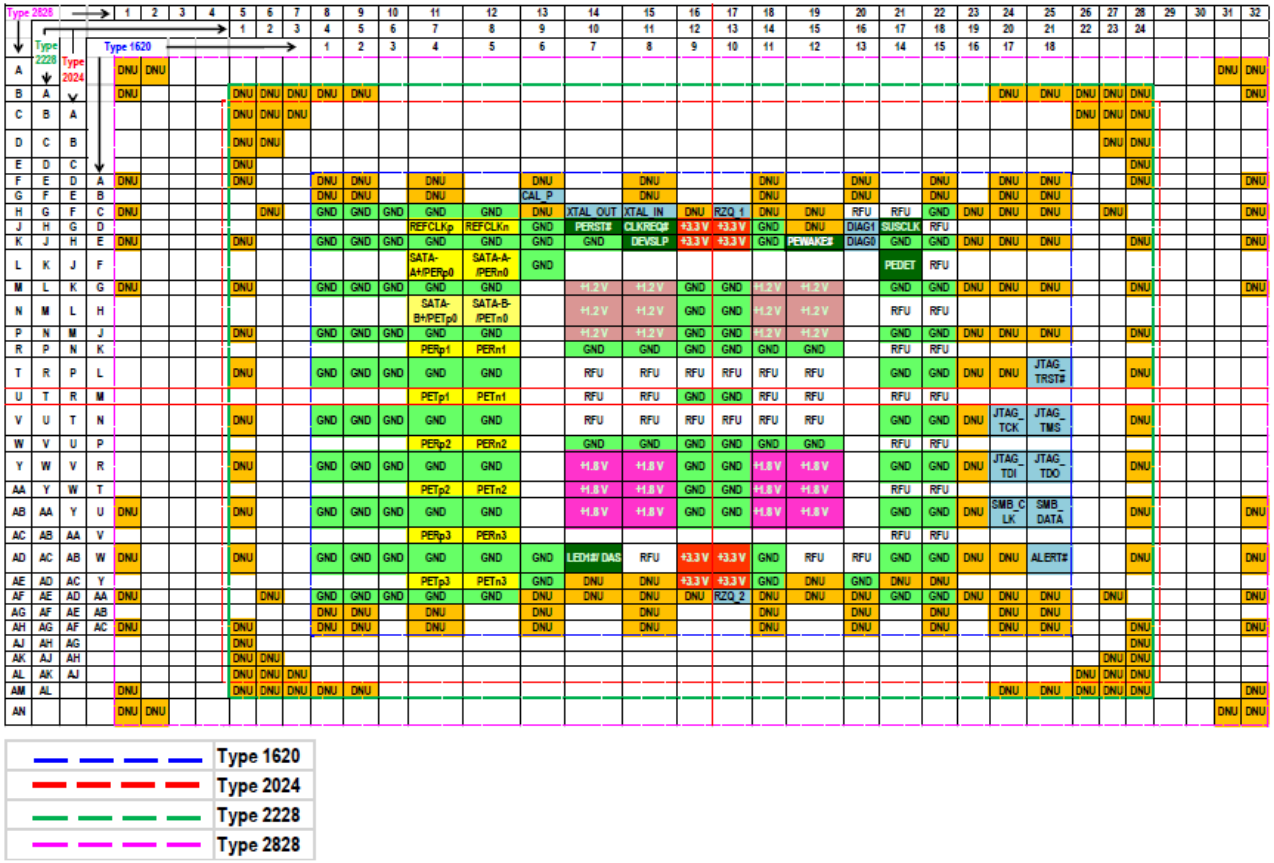


Figure 105. Type 1620 BGA Module-side Ballmap Surrounded by Type 2024, Type 2228, and Type 2828 Module-side Ballmaps (Top View)

Copyright © 2017 PCI-SIG® - All Rights Reserved

ECNs approved post Rev 1.1

- **11.5x13 mm SSD BGA ECN approved**
- **Enable PCIe and USB 3.0 on M.2 Card Key B ECN**

Copyright © 2017 PCI-SIG® - All Rights Reserved

11.5x13 mm BGA SSD ECN Key Deltas vs. the 16x20 mm BGA

- **<1/2 the size: 150mm^2 vs. 320mm^2**
 - Better fit in small form factor applications
- **Only supports x2 PCIe**
 - no x4 or SATA support
- **Inner balls are NC**
 - Allows for dual footprint of storage device with other mobile storage devices (eMMC and UFS)[1]
- **Optional SPI interface**
 - For optional NOR support

1. eMMC and UFS specs are managed by JEDEC

Copyright © 2017 PCI-SIG® - All Rights Reserved

Other Changes

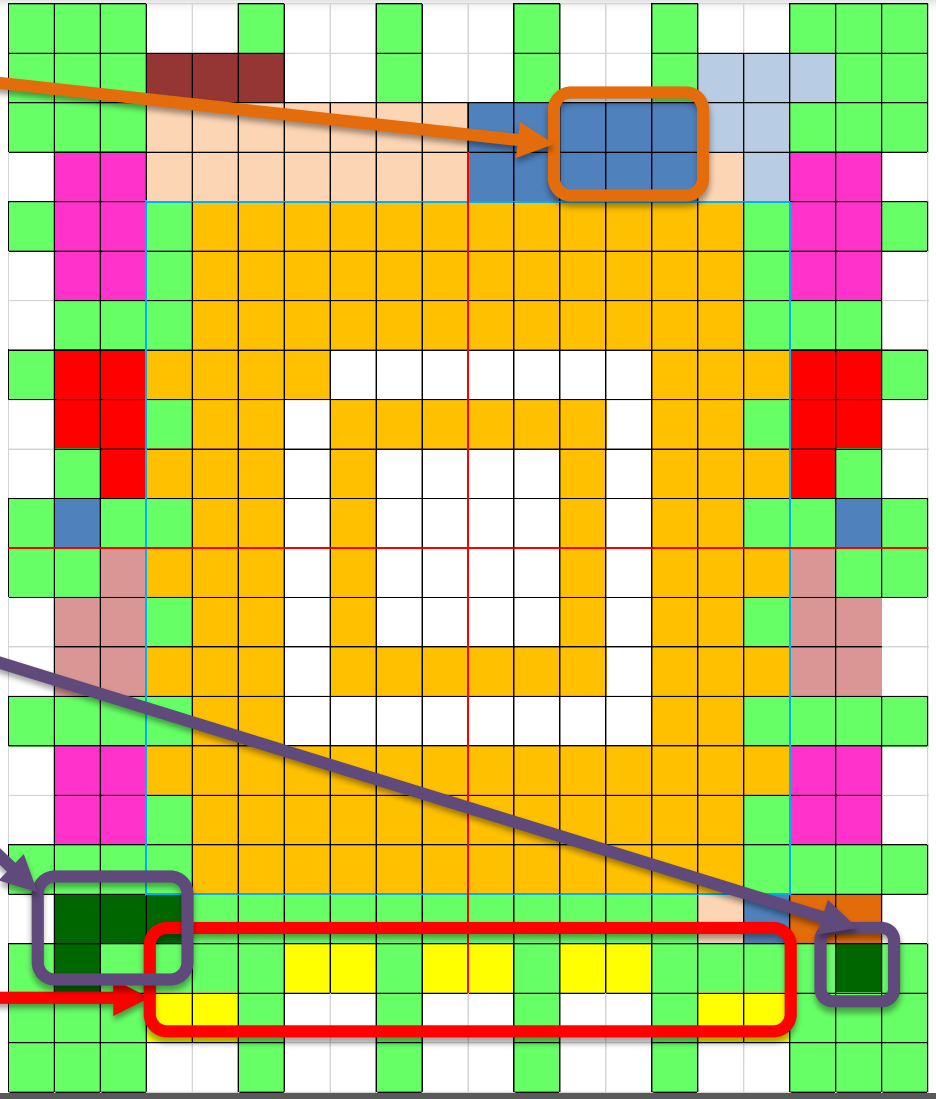
- **Multiple Voltage range support**
 - 16x20 spec introduced 3 voltages: 3.3 V, 1.8 V, and 1.2 V
 - 11.5x13 spec keeps 3 supplies but makes the power rail support device specific for flexibility.
 - Future ECN's could introduce additional voltages.

Pin Name (Nominal Voltage)	Voltage Range	Platform Rail Type
PWR_1 (+3.3 V)	2.8 V to 3.6 V	Always On
PWR_2 (+1.8 V)	1.7 V to 1.9 V	Always On
PWR_2 (+1.2 V) PWR_3 (+1.2 V)	1.14 V to 1.26 V	Always On
PWR_3 (+1.1 V)	1.06 V to 1.17 V	Always On
PWR_3 (+0.9 V)	0.86 V to 0.98 V	Always On

Copyright © 2017 PCI-SIG® - All Rights Reserved

Ballout Details -1

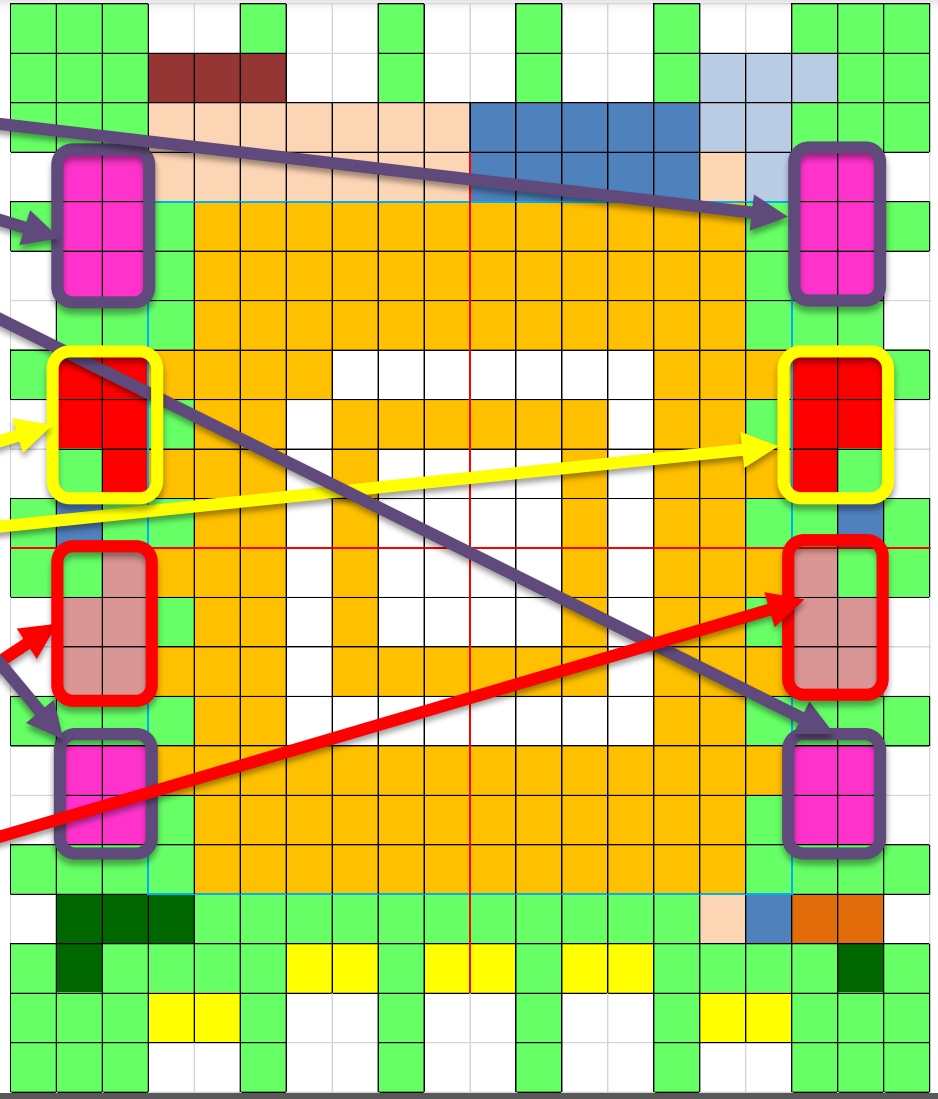
- **JTAG signals**
- **PCIe sideband**
- **PCIe lanes (x2)**



Copyright © 2017 PCI-SIG® - All Rights Reserved

Ballout Details -2

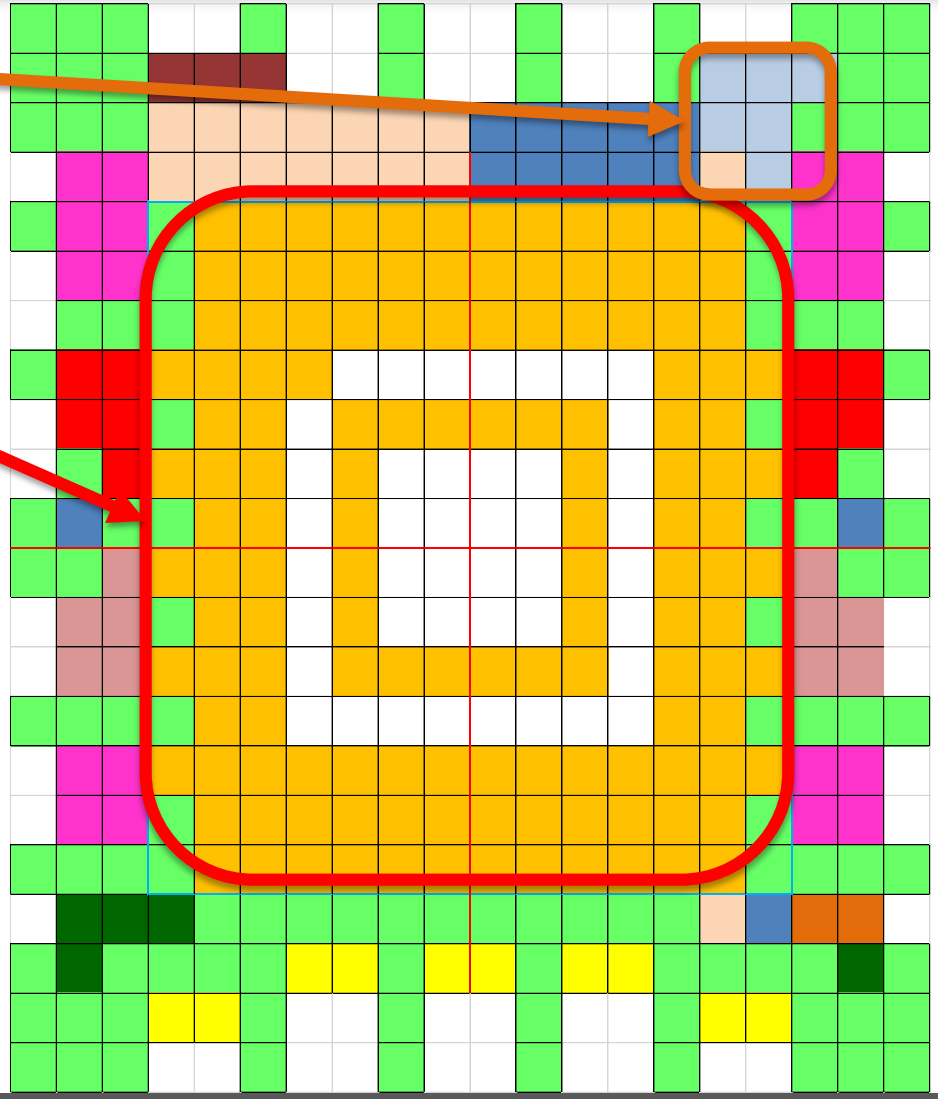
- **PWR_2**
- **PWR_1**
- **PWR_3**



Copyright © 2017 PCI-SIG® - All Rights Reserved

Ballout Details -3

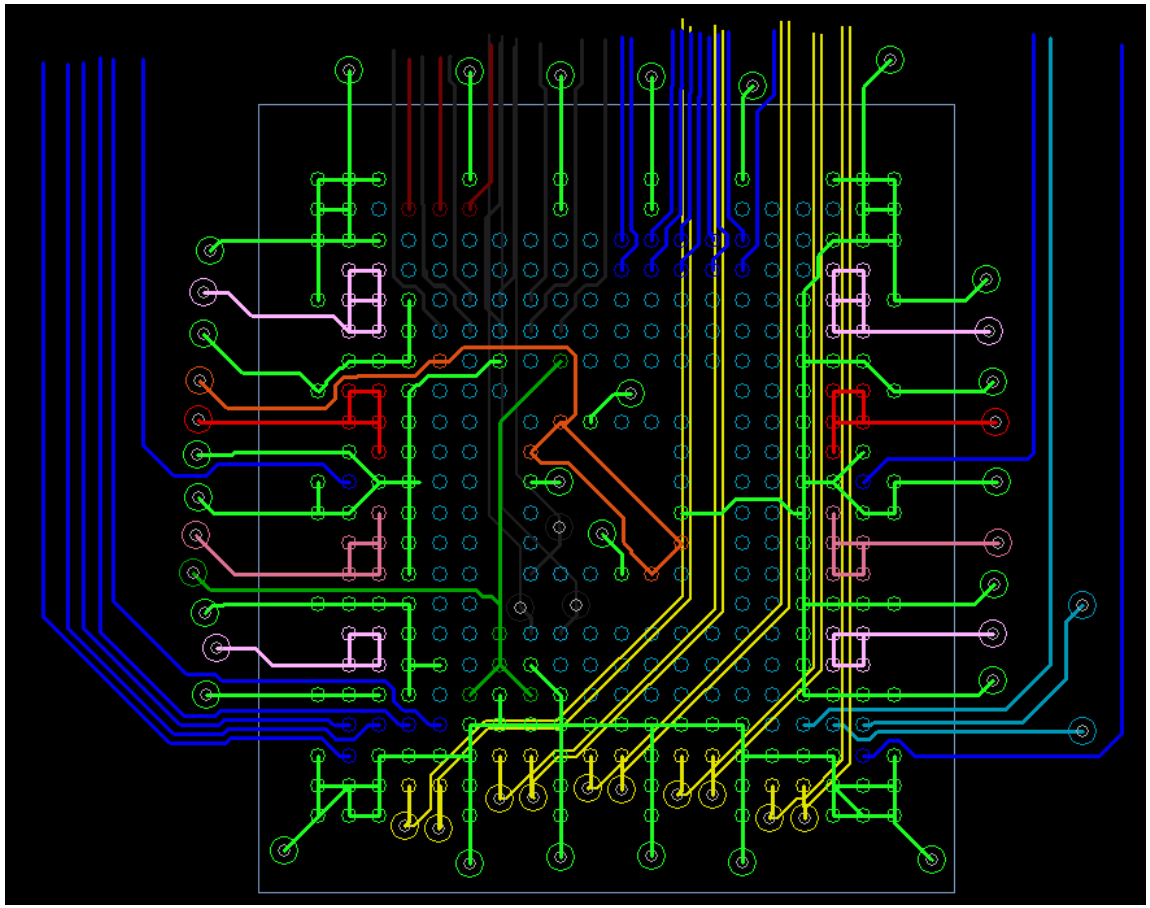
- **SPI Port (Optional)**
- **NC pins (along with a few grounds)**
 - This area can support other storage interfaces



Copyright © 2017 PCI-SIG® - All Rights Reserved

Routing Study

- **The ballout is friendly to Type 3 or Type 4 PCBs**



Copyright © 2017 PCI-SIG® - All Rights Reserved

Enable PCIe and USB 3.0 on M.2 Card Key B ECN

- **WWAN Key-B modified to enable PCIe and USB 3.1 Gen1 signals simultaneously**
- **Configuration States 4, 5, 6 and 7 modified**
- **Configuration State 14 re-defined**
- **Pinout tables updated to reflect the changes**

Copyright © 2017 PCI-SIG® - All Rights Reserved

Errata and Clarification

- **Typo's fixed in text and in figures**
- **Various Clarifications added**
 - **E.g. AC Coupling for PCIe, SATA and USB 3.0 differential signals**

Copyright © 2017 PCI-SIG® - All Rights Reserved



Mini CEM Updates

Copyright © 2017 PCI-SIG® - All Rights Reserved

PCIe Mini CEM Specification Updates

Incorporated the following ECNs and Errata:

- **PCIe_Base_r3_0_Errata_2014-10-23**
- **ECN_L1_PM_Substates_with_CLKREQ_31_May_2013**
- **Combined-Antenna-Tuning/Coexistence Signal ECN (May_31_2012)**
- **ECN- Add USB 3.0 to the Mini Card**
- **ECN- Tighten Mini Card Power Rail Voltage Tolerance**
- **Misc. changes from MiniCard_21_errata_table**

Copyright © 2017 PCI-SIG® - All Rights Reserved

Timeline

- **M.2 Specification Rev 1.1 was released on Dec 15, 2016**
- **Mini CEM Specification Rev 2.1 was released on Dec 15, 2016**

Copyright © 2017 PCI-SIG® - All Rights Reserved

Thank you for attending the PCI-SIG Developers Conference 2017.

For more information, please go to www.pcisig.com

Don't forget to submit your feedback via the mobile app!

Download the app by searching stores for **PCI-SIG Developers Conference** or entering the following URL into your mobile browser: **https://crowd.cc/s/EOtK**

Enter event code: **DevCon17**

Alternatively, access here: https://event.crowdcompass.com/devcon-17

Note: Create an account within the app so Admin knows who to contact if selected as the prize winner.

You will earn 1 raffle entry for each session you provide feedback on (up to 11 sessions).
General survey feedback = 1 raffle entry.

Copyright © 2017 PCI-SIG® - All Rights Reserved